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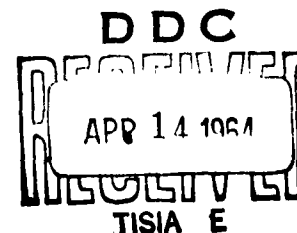
The Design of Wideband Transistor Amplifiers by an Extension of the Sampled-Parameter Technique

by
G. Danon and K. Sorenson

November 1963

Technical Report No. 4815-1

Prepared under
Office of Naval Research Contract
Nonr-225(24), NR 373 360
Jointly supported by the U.S. Army Signal Corps, the
U.S. Air Force, and the U.S. Navy
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Solid-State Electronics Laboratory
Stanford Electronics Laboratories
Stanford University Stanford, California

ABSTRACT

The experiments conducted in nuclear physics laboratories often require the design of fast-pulse amplifiers. Recent transistors offer new capabilities in this field. The work presented here centers on the design of such amplifiers by the sampled-parameter technique, in which the transistor is characterized by two-port parameters measured at a set of frequencies through the frequency band of interest. The feedback and coupling networks are selected by computations based on these sampled parameters. An application of this technique has led to an iterative stage using a 2N918 transistor and having the following characteristics:

1. Iterative impedance 50 ohms
2. Insertion power gain 10 db
3. Bandwidth 400 Mc
4. Rise time 1 nsec
5. Overshoot < 10 percent
6. Noise factor (throughout the band)..... 8-10 db
7. Output level, negative pulse -500 mv
8. Output level, positive pulse 200 mv

An amplifier of three such stages, cascaded, provided a gain of 30 db, a rise time of 1 nsec, and a bandwidth of 400 Mc.

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I. INTRODUCTION

A. PULSE AMPLIFIERS IN NUCLEAR PHYSICS

Experiments in high-energy physics have made necessary, in recent years, the design of amplifiers for faster and faster pulses. Such amplifiers are placed at the output of photomultipliers (Fig. 1) in order to drive a coincidence circuit, or, in some other experiments, the coincidence circuit is placed at the output of the photomultiplier while the pulse amplifier is supposed to realize the pulse shaping and the pulse amplifying before the signal goes to the scaler.

B. RECENT ADVANCES IN TRANSISTOR TECHNOLOGY

Until recently, only the vacuum tube could give a rise time of approximately 1 nsec. Recent advances in the transistor field make it possible for transistors to replace tubes advantageously. Some transistors with a maximum oscillation frequency greater than 2 Gc are now commercially available. Because of their small size, one can place, for some experiments, up to 10 or 12 transistor amplifiers very close to the scintillators, thus avoiding carrying a low-level signal along a 100-yard cable from the target area to the measurements area. Moreover, some recent work seems to indicate that the transistor behavior remains satisfactory even if it has been submitted to nuclear radiations for a "reasonable" length of time.

The above remarks explain why the electronics engineers in nuclear physics laboratories have been so deeply interested, among other things, in the design of wideband transistor amplifiers.

C. CONTINUOUS-WAVE RESPONSE AND PULSE RESPONSE

As is generally the case, this study was more concerned with bandwidth than pulse response. The reason for this is that it is very difficult to establish a link between desired output pulse characteristics and the location of transfer-function poles and zeros. Once the bandwidth is attained, the phase response can be modified by using an all-pass phase equalizer, as discussed by Fogarty [Ref. 1], or by modifying

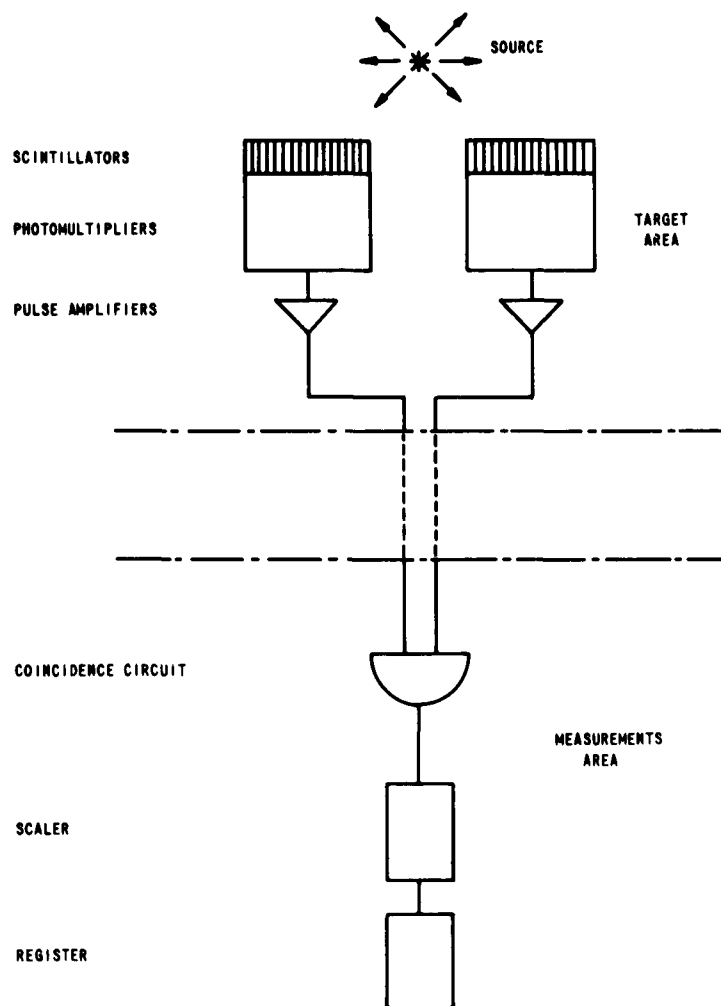


FIG. 1. ELECTRONIC APPARATUS FOR A NUCLEAR-PHYSICS EXPERIMENT.

the bandwidth experimentally. In the case of the 400-Mc, 1-nsec amplifier, it was not necessary to rely on these techniques, since the pulse overshoot (< 10 percent) was small enough for the intended application.

D. SOME RECENT ACHIEVEMENTS

Many pulse-amplifier designs are to be found in the literature. Some of the most notable results and the references reporting them are indicated below:

| <u>Reference Number</u> | <u>Transistor</u> | <u>Power Gain (db/stage)</u> | <u>Bandwidth (Mc)</u> |
|-----------------------------|---|----------------------------------|---------------------------|
| 2 | M 2039 Western Electric $f_T = 400 \text{ Mc}$ | 10 | 130 |
| 3 | 2N917 Fairchild $f_T = 800 \text{ Mc}$ | 6 | 2 nsec rise time |
| 4 | M 2107 Western Electric $f_T = 2 \text{ Gc}$ | 6 | 750 |
| 5 | M 2058 Western Electric $f_T = 550 \text{ Mc}$ | 7 | 200 |

E. TWO DIFFERENT POSSIBLE APPROACHES TO THE PROBLEM

Two main ways of approaching the problem are considered:

1. The transistor is represented by a model including R's, C's, and controlled sources. An attempt is made to determine the emitter current, the load and source impedances which give the maximum gain-bandwidth product, and the values of the associated circuit elements which correspond to a prescribed location for the poles of the transfer function (generally the "maximally flat" location).
2. The transistor is represented by a set of sampled matrix parameters, actually measured at a given value of emitter current. This procedure is J. G. Linvill's sampled-parameter method, the basic ideas of which are developed in Transistors and Active Circuits, by Linvill and Gibbons [Ref. 6].

The first method has the advantage of representing a physical system with a model: it allows a mathematical analysis and the associated circuit synthesis through the conventional techniques of network synthesis. It is also true, however, that this approach is only as good as the model, and generally raises the question of whether to use a simple model of limited validity or a more complex model requiring more complicated computations.

In the second approach the limitations on the validity of the transistor model pose no problem because one is operating directly on the measured transistor parameters. (See Fig. 2.) On the other hand, a set of matrix parameters can hardly be used as a guide in the choice of the type of associated circuits. It thus appears that good results may be achieved by combining the two approaches.

Linville's method consists in "roughing out" the problem with a very simple equivalent circuit. This first step leads to an appropriate circuit configuration and gives orders of magnitude for the gain and the bandwidth. A further step, using the sampled parameters, leads to more precise values.

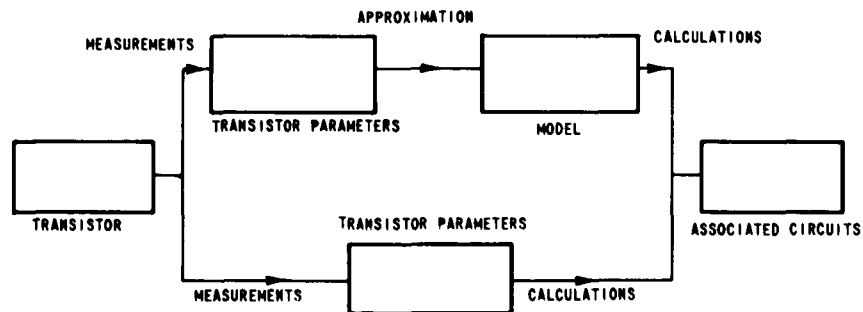


FIG. 2. TWO DIFFERENT APPROACHES TO THE DESIGN OF WIDEBAND AMPLIFIERS.

II. LINVILL'S LM CHART *

A. THE LM PLANE

The two-port parameters and terminal variables are related as follows:

$$I_1 = y_{11}E_1 + y_{12}E_2 \quad (1)$$

$$I_2 = y_{21}E_1 + y_{22}E_2 \quad (2)$$

It is convenient to consider a unit driving voltage:

$$E_1 = 1 + j0 \quad (3a)$$

The output voltage E_2 can be conveniently defined in terms of variables L and M in the following way. Moreover, the load admittance is found to be related to L and M .

$$E_2 = (L + jM) \frac{-y_{21}}{2y_{22r}} = -\frac{I_2}{Y_L} \quad (3b)$$

B. THE $P_0(L,M)$ PARABOLOID AND THE $P_1(L,M)$ PLANE

The output power

$$P_0 = \text{Re} (-E_2^* I_2) = L \frac{|y_{21}|^2}{2y_{22r}} - \frac{(L^2 + M^2)|y_{21}|^2}{4y_{22r}} \quad (4)$$

$P_0(L,M)$ is a paraboloid, and the coordinates of its summit are $(1,0)$ where P_0 is designated as P_{00} .

$$P_{00} = \frac{|y_{21}|^2}{4y_{22r}} \quad (5)$$

* The problem of selecting (by the sampled-parameter technique) source and load terminations of amplifiers to provide a realizable prescribed gain is discussed in Chapters 11, 18, and 19 of Transistors and Active Circuits [Ref. 6]. The reader is referred to that reference for background and details. The framework and notation of the reference is outlined in this section because subsequent development in this report extends the method.

The input power

$$P_i = \text{Re } E_1 I_1^* = y_{11r} + L \text{Re} \frac{-y_{12}y_{21}}{2y_{22r}} + M \text{Im} \frac{y_{12}y_{21}}{2y_{22r}} \quad (6)$$

$P_i(L, M)$ is an inclined plane. Its gradient line makes an angle θ with the L axis such that

$$\theta = -\arg(-y_{12}y_{21}) \quad (7)$$

$$\text{When } L = 1 \text{ and } M = 0, P_i = P_{i0} = \frac{2y_{11r}y_{22r} - \text{Re}(y_{12}y_{21})}{2y_{22r}} \quad (8)$$

The coordinates $L = 1, M = 0$ correspond to

$$Y_L = y_{22}^* \quad P_i = P_{i0} \quad P_o = P_{o0} \quad (9)$$

The two-port is potentially unstable when $(P_{o0}/P_{i0}) < 0$, or when the critical factor

$$C = \frac{2P_{o0}}{P_{i0}} \left| \frac{y_{12}}{y_{21}} \right| > 1 \quad (10)$$

Moreover, when $C < 1$, the maximum available gain ($Y_s = Y_{in}^*$ and $Y_L = Y_o^*$) is never larger than $2(P_{o0}/P_{i0})$.

C. THE LOAD ADMITTANCE (Y_L) IN THE LM PLANE

The load admittance is found to be

$$Y_L = -y_{22} + \frac{2y_{22r}}{L + jM} \quad (11)$$

and $G + jB$ is defined in the following way:

$$Y_L + y_{22} = \frac{2y_{22r}}{L + jM} = G + jB \quad (12)$$

Thus a load admittance Y_L is determined by any one of three sets of coordinates-- (Y_{Lr}, Y_{Li}) , (L, M) , or (G, B) , and we can draw in the LM plane the constant G and the constant B circles. The chart thus obtained (Fig. 3) is a very simplified version of Linvill's chart but it contains all the elements which will be needed for the particular purpose of this discussion.

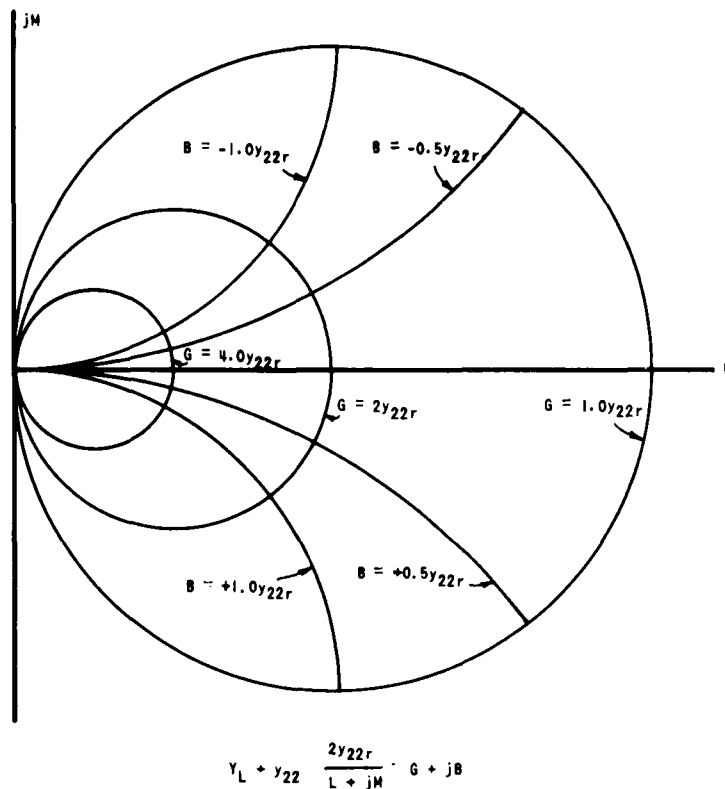


FIG. 3. LOAD ADMITTANCE IN THE LM PLANE.

D. THE CONSTANT-g CIRCLES

From the charts shown in Fig. 4 two new axes, x and y , are chosen such that their origin lies at $L = 1$, $M = 0$, and such that their angles with the L axis are θ and $\theta + (\pi/2)$.

The locus of points for which $g = (P_0/P_{00})/(P_1/P_{10})$ is constant is a circle:

$$1 - g(1 + Cx) = x^2 + y^2 \quad (13)$$

The circles which correspond to different values of g have two points in common if $C > 1$ (Fig. 4a), and no point in common if $C < 1$ (Fig. 4b).

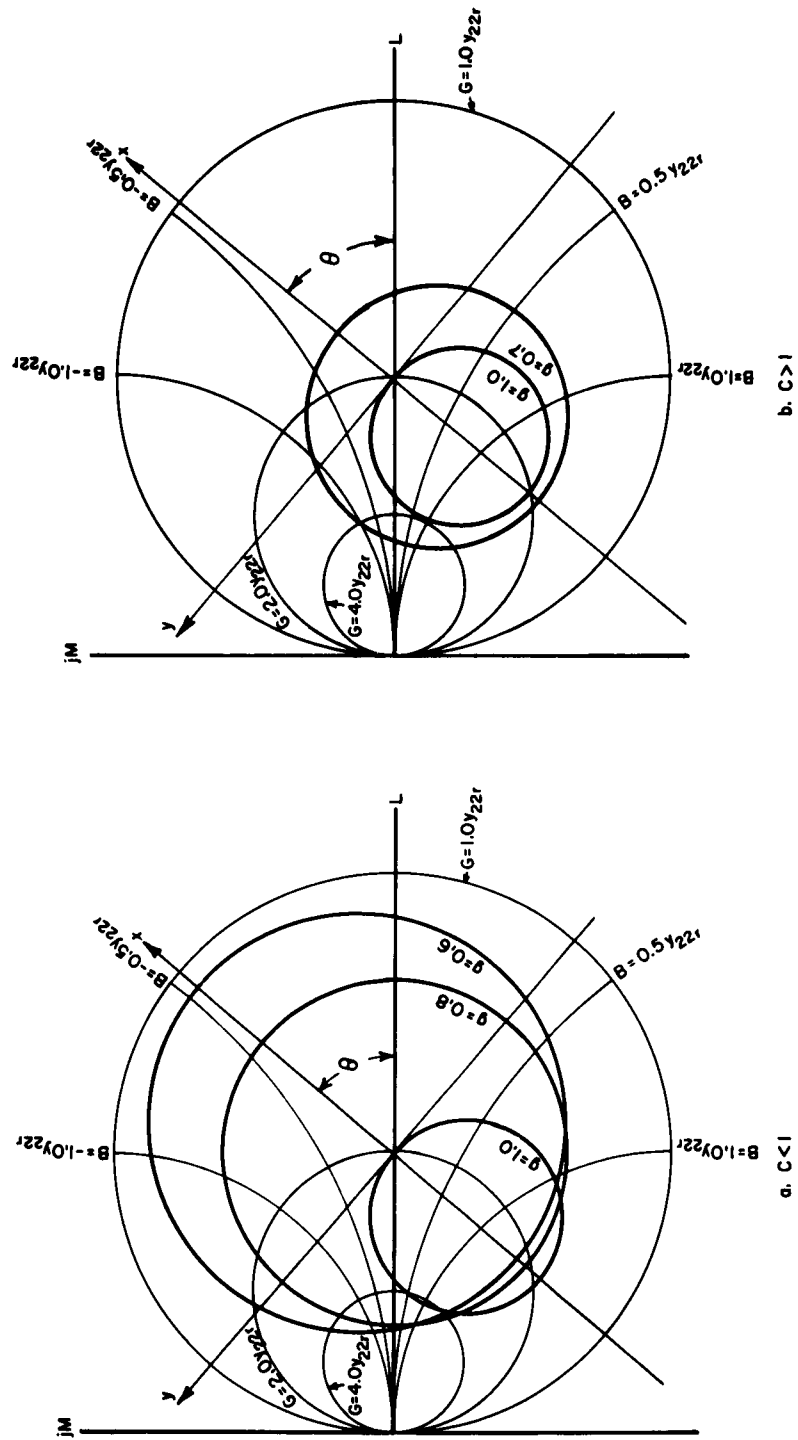


FIG. 4. LOCUS OF CONSTANT POWER GAIN, $g = (P_o/P_{o0}) / (P_i/P_{i0})$.

III. THE R-L COLLECTOR-TO-BASE FEEDBACK

The first step in the design of a broadband amplifier can now be undertaken. With a given transistor, a simple equivalent circuit will be used in order to determine approximately the power gain per stage, the bandwidth, and the elements of the electrical circuits.

A. AN EQUIVALENT CIRCUIT FOR THE 2N918 TRANSISTOR

The 2N918, which is used in the broadband amplifier, is a Fairchild NPN silicon, planar epitaxial, double-diffused transistor. (Total maximum power dissipation = 200 mw at 25 °C ambient, $V_{CBO} = 30$ v, and $I_{C\text{ max}} = 50$ ma.) Table 1 lists the sampled y parameters of this transistor as they can be inferred from the Fairchild data sheet of May, 1962. (The 10-Mc parameters have been added.)

TABLE 1. SAMPLED y PARAMETERS OF THE FAIRCHILD 2N918 TRANSISTOR
($I_E = 5$ ma, $V_{CE} = 10.0$ v)

| f (Mc) | Parameter (mmho) | | | |
|-----------|------------------|-----------------|----------------|----------------|
| | y_{11} | y_{12} | y_{21} | y_{22} |
| 10 | $1.7 + j0.65$ | $-0.01 - j0.07$ | See Footnote | $0.08 + j0.13$ |
| 50 | $2.5 + j2.5$ | $0.00 - j0.3$ | $80.0 - j60.0$ | $0.1 + j1.0$ |
| 100 | $5.0 + j5.0$ | $0.00 - j0.7$ | $40.0 - j60.0$ | $0.2 + j1.3$ |
| 200 | $8.0 + j8.0$ | $0.00 - j1.3$ | $25.0 - j55.0$ | $0.5 + j2.5$ |
| 300 | $10.0 + j10.0$ | $-0.1 - j2.0$ | $15.0 - j47.0$ | $0.6 + j3.5$ |
| 400 | $12.0 + j12.0$ | $-0.2 - j2.7$ | $7.0 - j43.0$ | $0.8 + j4.5$ |
| 500 | $17.0 + j14.0$ | $-0.4 - j3.4$ | $0.0 - j40.0$ | $1.0 + j6.0$ |

* $g_m = 100.0 + j40.0$ at 10 Mc.

Reading this table makes an important fact apparent: While $y_{12i}(f)$ is approximately a linear function of frequency, $y_{12r}(f)$ is approximately a parabolic function. This fact suggests that a π equivalent circuit (Fig. 5) can be used, the feedback admittance being an r_C - C_C series circuit with $r_C C_C \omega < 1$.

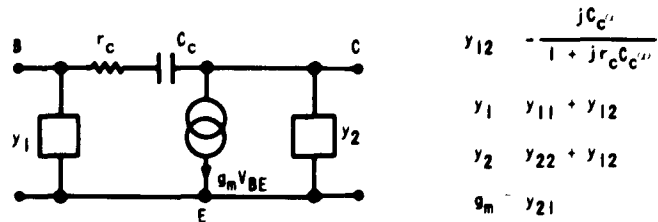


FIG. 5. A π EQUIVALENT CIRCUIT FOR THE 2N918 TRANSISTOR.

For such a circuit the following expression can be written:

$$-y_{12} = \frac{jC_c\omega}{1 + jr_c C_c\omega} \approx r_c C_c \omega^2 + jC_c\omega \quad (14)$$

By comparison of the above expression with the parameters in Table 1, one can calculate that:

$$C_c = 1 \text{ pf} \quad r_c = 30 \text{ ohms} \quad (15)$$

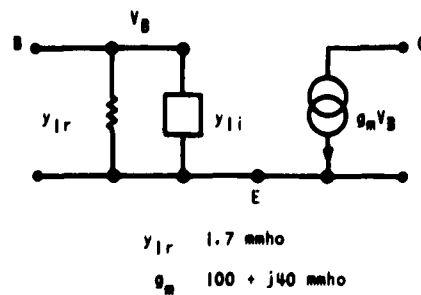
At a very low frequency ($f = 10 \text{ Mc}$), the transistor can be represented by the circuit shown in Fig. 6.

At high frequencies, the transistor can be represented by the circuit in Fig. 7, in which

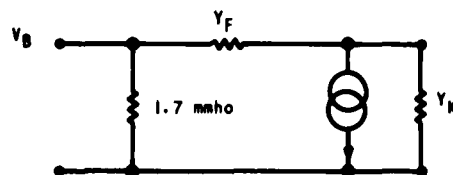
$$y_1 = y_{1r} + jy_{1i} = y_{11} + y_{12} \quad (16)$$

$$y_2 = y_{2r} + jy_{2i} = y_{22} + y_{12} \quad (17)$$

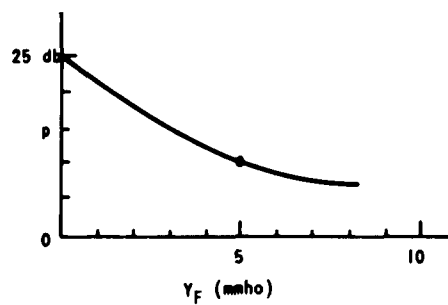
and g_m is complex. The parameters y_{1r} and y_{2r} can be computed from Table 1 in Sec. IIIA. The parameters y_{1i} and y_{2i} need not be calculated since they do not influence the value of (P_{o0}/P_{i0}) .



a. The equivalent circuit at 10 Mc

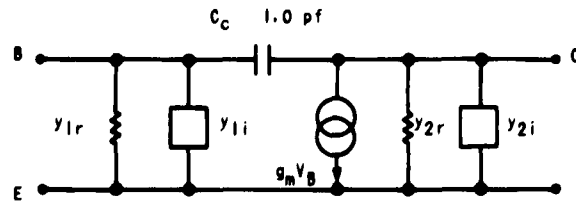


b. The equivalent circuit with feedback at 10 Mc

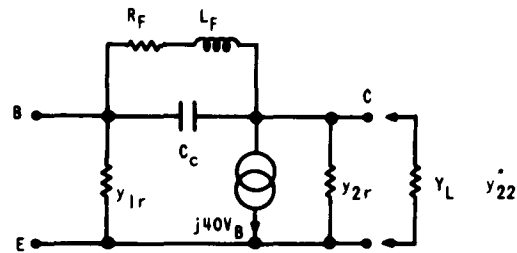


c. Power gain p vs Y_F at 10 Mc

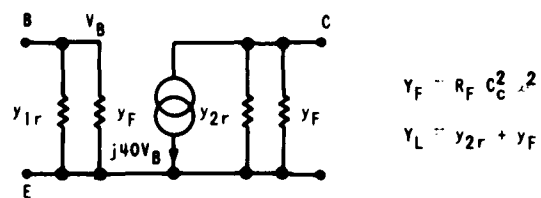
FIG. 6. TRANSISTOR MODEL FOR A FREQUENCY OF 10 Mc.



a. An equivalent circuit for the 2N918 transistor without external feedback



b. Tuning C_c by means of external feedback



c. Resultant equivalent circuit at amplifier cutoff frequency ω_c

FIG. 7. TRANSISTOR MODEL FOR HIGH FREQUENCIES.

B. THE INFLUENCE OF COLLECTOR-TO-BASE FEEDBACK

The influence of feedback at a low frequency (10Mc) is considered first. In the circuit of Fig. 6b, Y_K is the load conductance. (At low frequencies the characteristic admittance $Y_K =$ the load admittance Y_L .) Y_F is the feedback conductance ($1 < Y_F < 10$ mmho), and $p(Y_K, Y_F)$ is the power gain of the stage (Fig. 6b). Choosing, for example, $Y_K = 20$ mmho, we can plot $p(Y_F)$ as shown in Fig. 6c.

It can be seen that when the stage is loaded with 50 ohms, a 200-ohm feedback resistor from collector to base will reduce the gain to 10 db, while the input impedance will come close to 50 ohms. Thus it seems feasible (at least at low frequencies) to design a 50-ohm iterative stage. The maximum bandwidth which can be expected is determined next. From the equivalent circuit shown in Fig. 7, the values of y_{1r} and y_{2r} for frequencies between 200 and 500 Mc are obtained (see Table 2).

TABLE 2. VALUES OF y_{1r} AND y_{2r} FOR THE 2N918 TRANSISTOR

| Parameter (mmho) | Frequency (Mc) | | | |
|---------------------|----------------|-----|-----|-----|
| | 200 | 300 | 400 | 500 |
| y_{1r} | 8 | 10 | 12 | 17 |
| y_{2r} | 0.5 | 0.5 | 0.6 | 0.6 |

Now $C_C = 1$ pf is tuned with an R_F - L_F series circuit ($R_F = 200$ ohms), and Y_L is chosen such that $Y_L = y_{22}^*$ (Fig. 7b). The stage power gain now nears the maximum value that can be expected with a given R_F (determined by the low-frequency requirements). To calculate this maximum value, note that C_C , R_F , and L_F make a resonant circuit which can be replaced by a conductance $R_F C_C^2 \omega_C^2$, ω_C being the cutoff frequency of the amplifier to be determined. This conductance does not modify y_{21} appreciably, but it does modify y_{22} and y_{11} . Moreover, within the frequency range of 200 to 500 Mc, $y_{21} \approx -j40$, the "Miller effect" does not modify $y_{in r}$, and thus the conductance $R_F C_C \omega_C^2$ can be removed and merely placed in parallel with y_{2r} and with y_{1r} (Fig. 7c).

Table 3 contains the results of calculating

$$y'_{1r} = y_{1r} + y_F \quad (18)$$

$$y'_{2r} = y_{2r} + y_F \quad (19)$$

and the corresponding value of (P_{o0}/P_{i0}) , Y_L having been chosen such that $Y_L = y'_{2r}$

$$\frac{P_{o0}}{P_{i0}} = \frac{|y_{21}|^2}{4y_{11r}y_{22r} - 2\text{Re}(y_{12}y_{21})} \approx \frac{400}{y'_{1r}y'_{2r}} \quad (20)$$

TABLE 3. COMPUTED VALUES OF y'_{1r} , y'_{2r} , AND P_{o0}/P_{i0}

| Parameter | Frequency (Mc) | | | |
|------------------------------|----------------|------|------|-----|
| | 200 | 300 | 400 | 500 |
| y'_{1r} (mmho) | 8.3 | 10.8 | 13.2 | 19 |
| y'_{2r} (mmho) | 0.8 | 1.3 | 1.8 | 2.6 |
| $\frac{P_{o0}}{P_{i0}}$ (db) | 18 | 14.5 | 12 | 9 |

From the above table it is seen that a 10-db power gain up to about 400 Mc can be expected. For this cutoff frequency, the tuning inductance $L_F = 160$ nh and the input impedance is approximately 76 ohms. ($y'_{1r} = 13.2$ mmho). When used in a 50-ohm system the power loss resulting from mismatch at the input would be less than 0.2 db, provided that an appropriate output coupling is designed.

Thus, a very simple equivalent circuit has provided orders of magnitude for R_F (200 ohms), L_F (160 nh), for the gain-bandwidth product (1200 Mc), and for the characteristic impedance (50 ohms). But it is still not known what the frequency response will be between $f = 0$ and $f = 400$ Mc. For a given transistor and feedback network, the response will depend mainly on the interstage filter. However, for a given interstage filter, it is possible to vary the frequency response by modifying the feedback circuit.

The following observations can be made on the basis of what has already been learned from the equivalent circuit.

1. A frequency-response curve similar to that represented in Fig. 8a can be smoothed with two inductors in the feedback circuit, one being a ferrite coil and the other an air coil (Fig. 8b). While the air coil tunes C_C at 400 Mc, the ferrite coil tunes C_C at a lower frequency f_1 , the material being chosen such that the corresponding inductance is negligible at 400 Mc.
2. A frequency-response curve similar to that represented in Fig. 8c can be smoothed with a parallel damping resistor R_D .

The foregoing ideas based on the transistor equivalent circuit were not developed mathematically. Qualitative considerations of those ideas, however, were very helpful during the experimental step of our procedure.

C. THE CONSTANT- (P_{o0}/P_{i0}) CIRCLES

The second step in the computations will lead to more precise values for L_F , R_F , the maximum gain-bandwidth product, and to the design of the interstage two-port.

Consider again the expression for (P_{o0}/P_{i0}) [Ref. 6, p. 248]:

$$\frac{P_{o0}}{P_{i0}} = \frac{|y_{21}|^2}{4y_{11r}y_{22r} - 2 \operatorname{Re}(y_{12}y_{21})} \quad (21)$$

In this relation, $[y]$ is the matrix of a two-port which is shunted by an R_F - L_F circuit (Fig. 9). That is,

$$[y] = [y_T] + [y_F] \quad (22)$$

where

$$[y_F] = \begin{bmatrix} y_F & -y_F \\ -y_F & y_F \end{bmatrix} \quad (23)$$

and

$$y_F = \frac{1}{R_F + jL_F} = g_F + jb_F \quad (24)$$

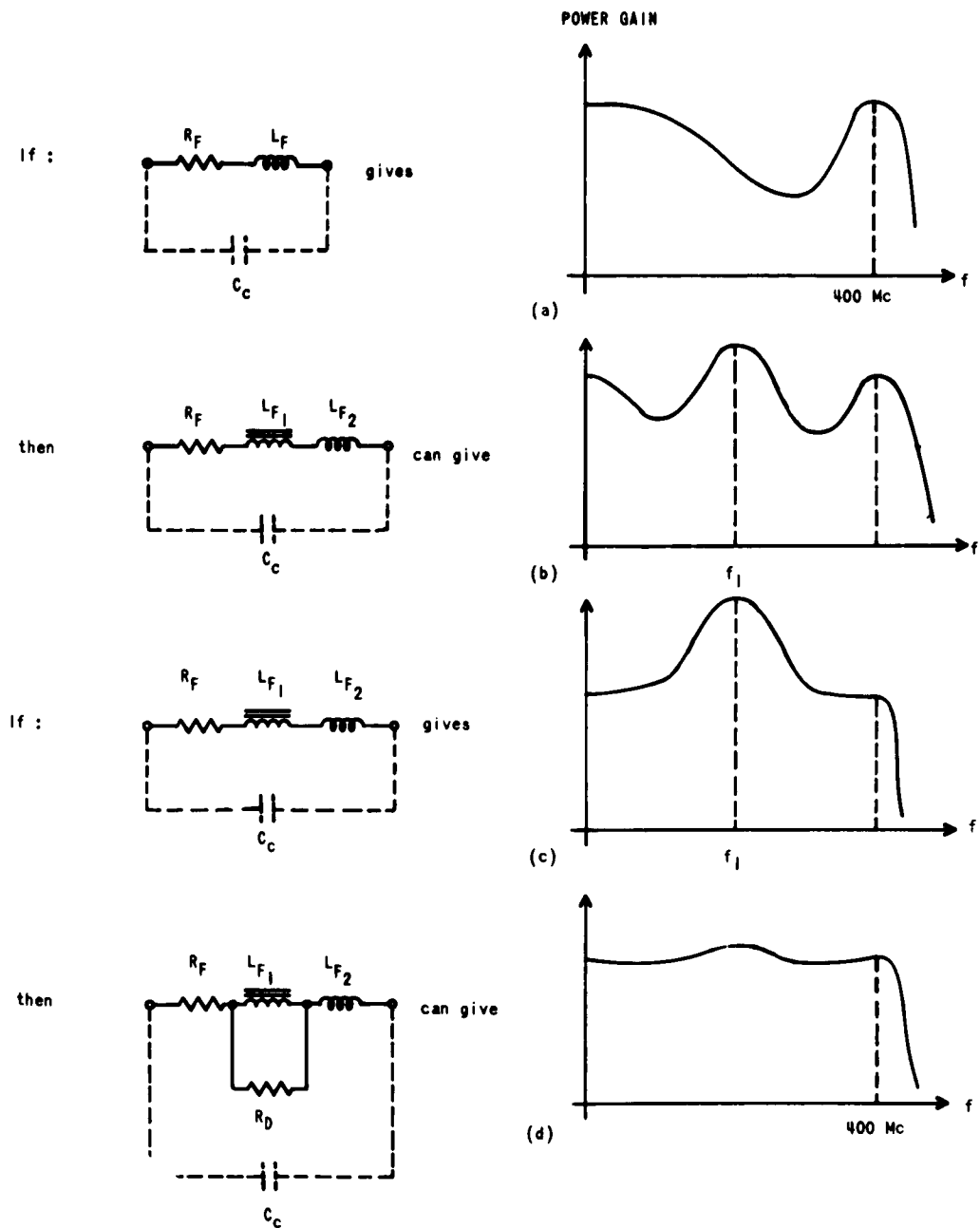


FIG. 8. FREQUENCY RESPONSE CONSIDERING COLLECTOR-TO-BASE FEEDBACK ONLY.

Thus,

$$\begin{aligned}
 \frac{P_{O0}}{P_{i0}} &= \frac{|y_{21T} - g_F - jb_F|^2}{4(y_{11rT} + g_F)(y_{22rT} + g_F) - 2 \operatorname{Re}(y_{12T} - y_F)(y_{21T} - y_F)} \\
 &= \frac{(y_{21rT} - g_F)^2 + (y_{21iT} - b_F)^2}{4(y_{11rT} + g_F)(y_{22rT} + g_F) - 2\{(y_{12rT} - g_F)(y_{21rT} - g_F) - (y_{12iT} - b_F)(y_{21iT} - b_F)\}}
 \end{aligned}
 \tag{25}$$

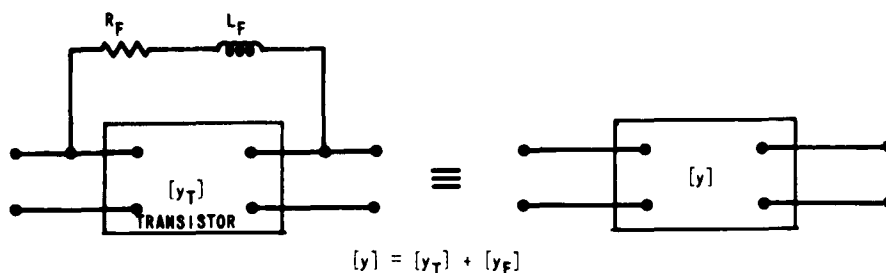


FIG. 9. MATRIX OF A TRANSISTOR SHUNTED BY AN R_F - L_F CIRCUIT.

For a given value of $(P_{O0}/P_{i0}) = p$, the above relation is the equation of a circle. This fact suggests a simple method of determining R_F , L_F , and p . Consider, on a Smith chart (Fig. 10), the constant R_F circles. For each of these values of R_F (Fig. 6c), there is one value for p (low-frequency power gain with a given value of Y_K). The constant (P_{O0}/P_{i0}) circles can be drawn on the same chart. For a given desired power gain p , R_F must be simultaneously on the two corresponding circles. Figure 10 clearly shows that the highest value for p corresponds to two tangent circles and that any lower value will lead to two values for R_F (and L_F).

Thus, for a given value of Y_K , knowledge of the y parameters at a very low frequency f_0 and the y parameters at any other frequency f leads, in a straightforward way, to an estimation of the maximum power gain (within 3 db) which can be expected from a video amplifier having a bandwidth $B = f - f_0$, and to knowledge of the R_F - L_F feedback circuit.

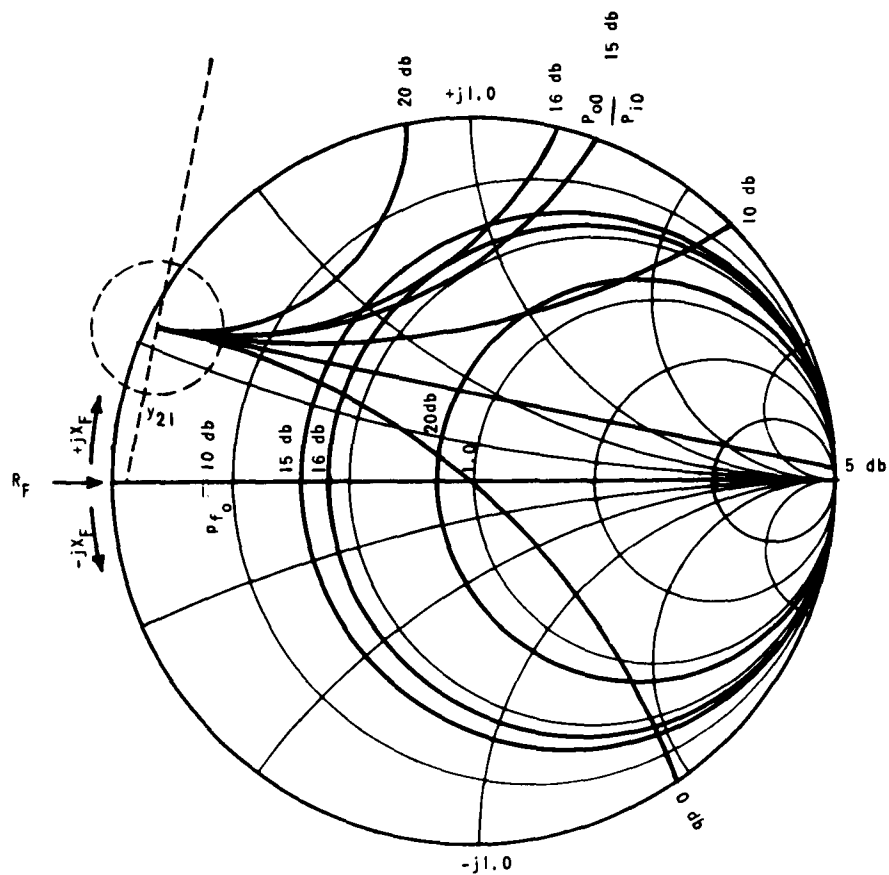


FIG. 10. SUPERPOSITION OF THE CONSTANT LOW-FREQUENCY AND HIGH-FREQUENCY POWER-GAIN CIRCLES. In this illustration the highest value for the power gain, p_{\max} , corresponds to the two tangent circles for which $p = 16$ db.

IV. DETERMINATION OF $Y_L(f)$ AND THE INTERSTAGE NETWORK

A. THE MAPPING OF Y_L : CONSTANT- ρ CIRCLES AND CONSTANT- p CIRCLES

At this point, R_F and L_F are known, and for a required bandwidth B , the maximum power gain p which can be expected with a given load admittance $Y_L = Y_K$ is also known. The transistor with its feedback circuit now behaves like a new transistor, characterized by y parameters for a set of sampled frequencies. The following question shall now be answered. How can the interstage filter be designed in order to achieve, in the band B (Fig. 11), a constant input admittance $Y_{in} = Y_K$, and a constant power gain p ?

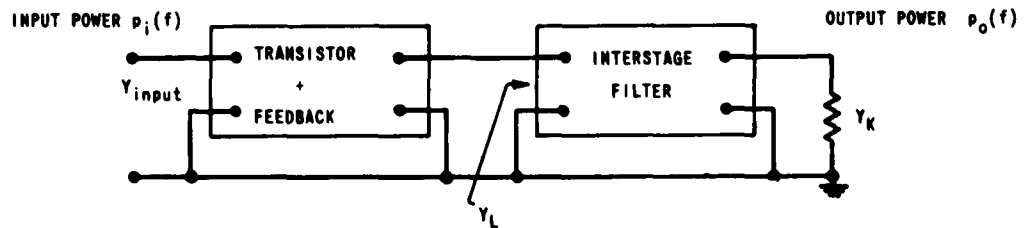


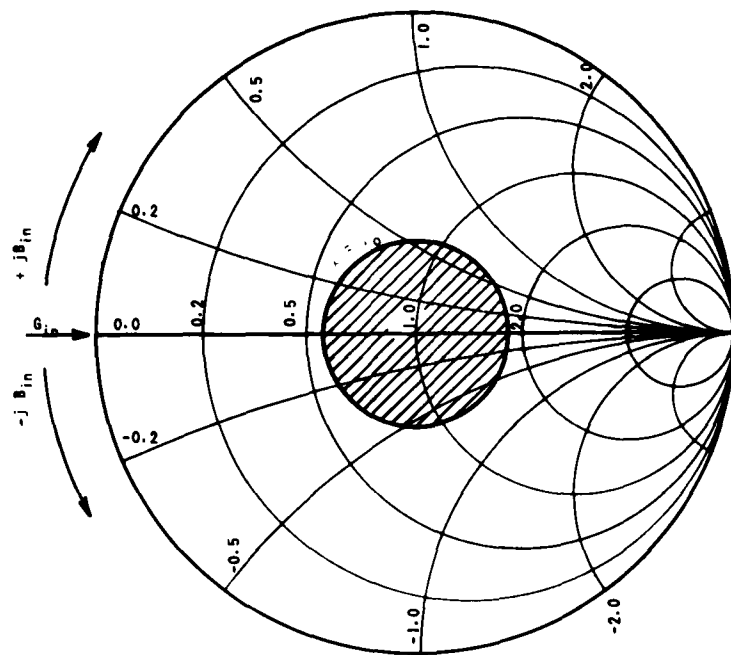
FIG. 11. BLOCK DIAGRAM OF THE COMPLETE AMPLIFIER STAGE. The general requirements are that $Y_{input} = Y_K$ and $P_o/P_i = p$.

1. The Input-Admittance Requirement

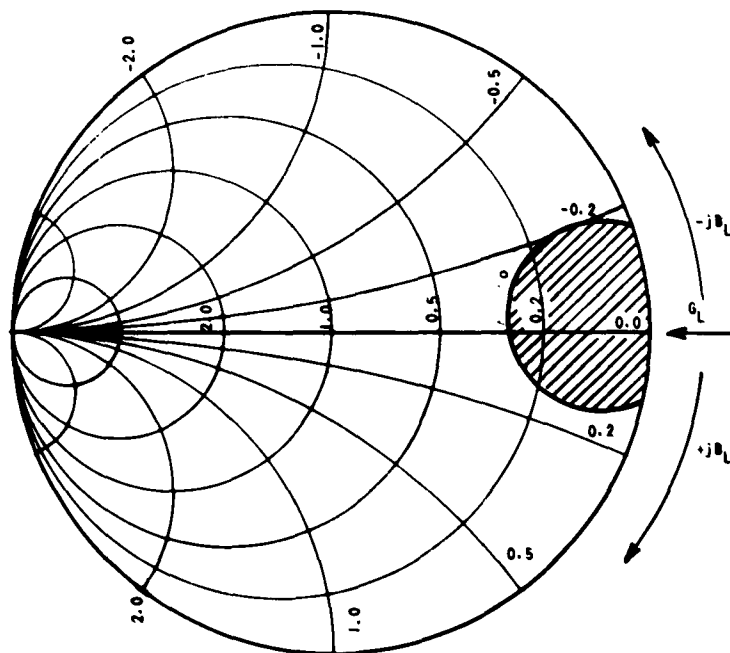
An arbitrary value ρ_o is chosen for the input reflection coefficient, and the new requirement on the input admittance Y_{in} is formulated by stating that, for any frequency, the input admittance of the amplifier must lie on a Smith chart, inside the constant ρ_o circle. But it is known that Y_{in} is related to Y_L in the following way:

$$Y_L = -y_{22} - \frac{y_{12}y_{21}}{Y_{in} - y_{11}} \quad (26)$$

Thus, two circles that correspond to each other can be drawn on two separate Smith charts (Fig. 12), one for the input admittance and one



a. Input admittance chart. The shaded region is the locus of Y_{in} for any input reflection coefficient $|\Gamma| \leq 0.5$.



b. Load admittance chart. The shaded region is the locus of Y_L for any input reflection coefficient $|\Gamma| \leq 0.5$.

FIG. 12. THE INPUT AND LOAD ADMITTANCE REQUIREMENTS.

for the load admittance. For any load admittance inside the right shaded circle, the transistor will present an input reflection coefficient less than ρ_0 .

2. The Power-Gain Requirement

It is specified that within the band B, the stage power gain must not differ from p by more than Δp . That is,

$$p - \Delta p \leq \text{stage power gain} \leq p + \Delta p$$

But it is known that on the LM plane, and consequently on a Smith chart (Fig. 13), the load admittances Y_L that provide power gains $p - \Delta p$ and $p + \Delta p$ are located on two circles. The load admittances that provide power gains between those two values are to be found between those two circles.

If both the input-admittance requirement and the power-gain requirement are to be taken into account simultaneously, Y_L must be chosen inside the region that belongs to the two regions just specified. This region will be the permissible region for Y_L at a frequency f (Fig. 14).

Proceeding in the same way for each sampled frequency leads to as many permissible regions as there are sampled frequencies. These regions will be drawn on a single Smith chart (Fig. 15), or more effectively, on two superimposed reversed Smith charts, as shown in Fig. 20. (See also Chapter 14 of Ref. 6.)

B. THE INTERSTAGE NETWORK

The interstage network (Fig. 11) transforms Y_K into $Y_L(f)$. A ladder type, nondissipative filter will be chosen. Usually a single π (or a T) section will give satisfactory results (Fig. 16). Although some advanced mathematical methods are available for the design of such a ladder [Ref. 6, Chap. 14], experience shows that a few trials on the Smith chart will bring the input admittances at the different frequencies inside the corresponding permissible regions. Finally one arrives at the stage represented in Fig. 17. It will be found later that, for the 400-Mc amplifier, the interstage filter can be reduced to a single inductor. The design and realization of such an amplifier will be considered in the next chapter.

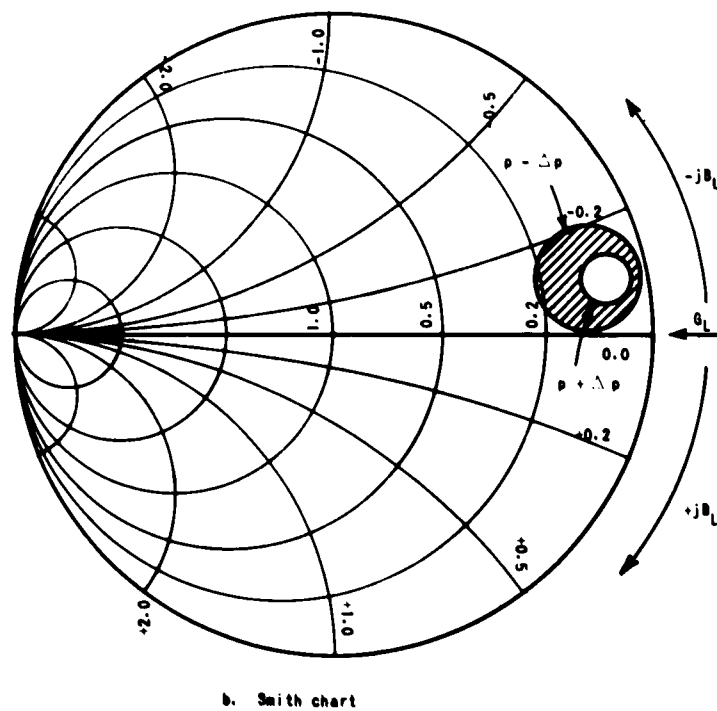
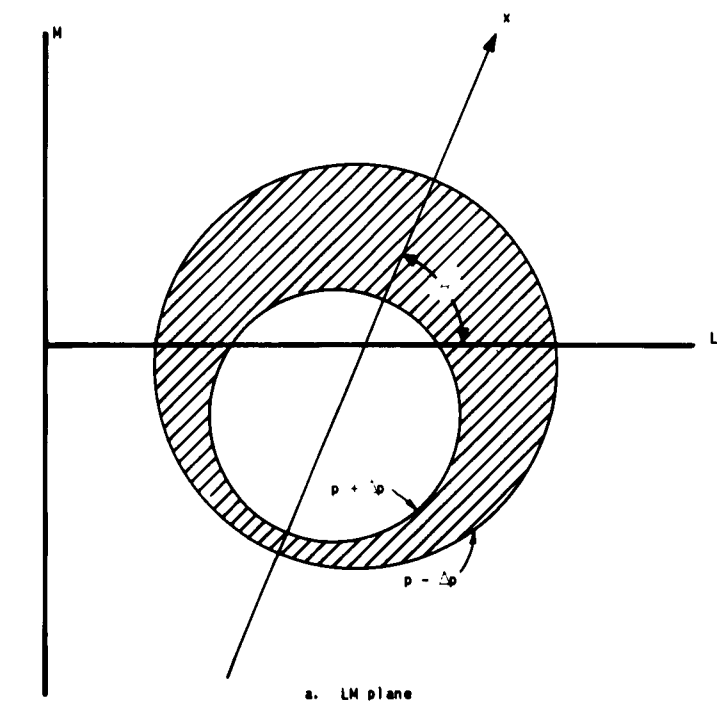


FIG. 13. THE POWER-GAIN REQUIREMENTS. The shaded regions are the loci of power gains between $p - \Delta p$ and $p + \Delta p$.

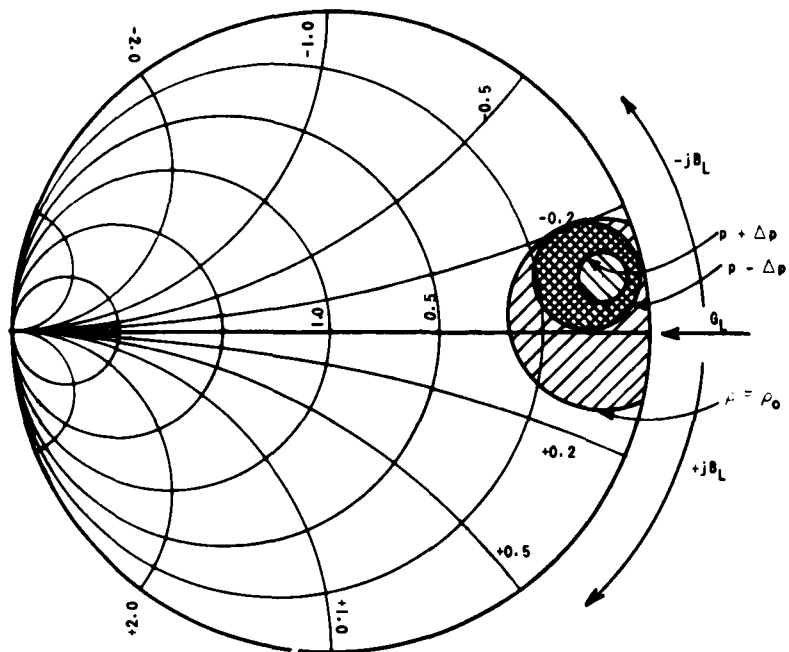


FIG. 14. THE PERMISSIBLE REGION FOR Y_L AT A GIVEN FREQUENCY. To meet the requirements on both power gain and input admittance, Y_L must be located in the shaded region.

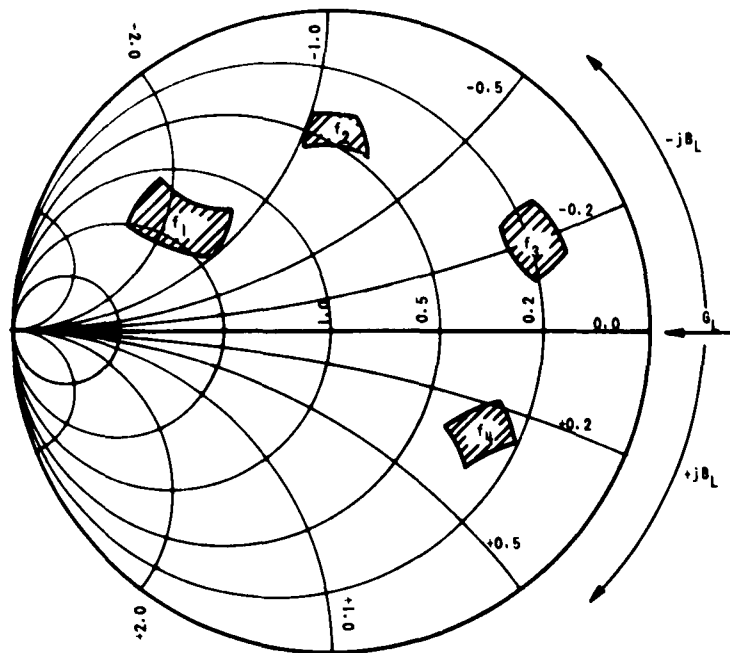


FIG. 15. THE PERMISSIBLE REGIONS FOR Y_L FOR SEVERAL FREQUENCIES. The interstage network transforms Y_K into $Y_L(f)$ such that for the sampled frequencies $f_1, f_2, f_3, f_4, \dots$, Y_L 's image on the chart comes into the corresponding shaded region.

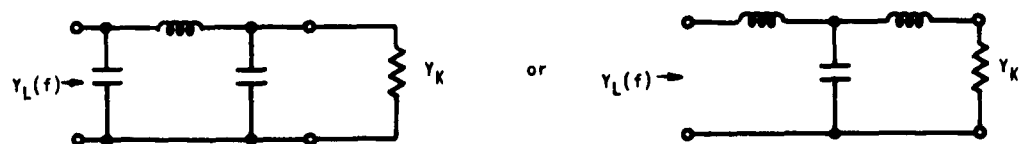


FIG. 16. THE INTERSTAGE NETWORK.

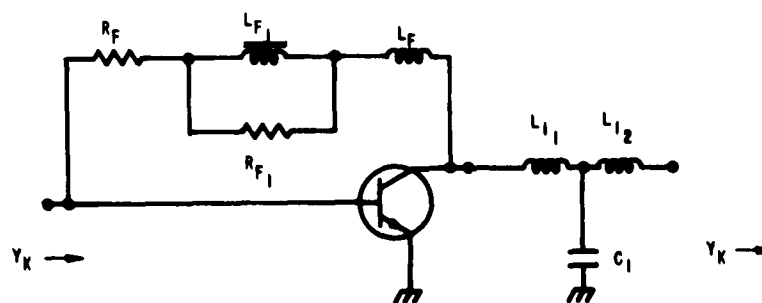


FIG. 17. AN ITERATIVE SINGLE-STAGE AMPLIFIER.

V. A 400-Mc, 30-db TRANSISTOR AMPLIFIER

A. THE STEP-BY-STEP PROCEDURE

The step-by-step procedure leading to the design of a 400-Mc, 30-db transistor amplifier is now presented.

1. The 2N918 y Parameters

In Table 4 the sampled y parameters of the 2N918 transistor are restated for reference purposes.

TABLE 4. RESTATEMENT OF THE SAMPLED y PARAMETERS OF THE
2N918 TRANSISTOR, $[Y_T](f)$
($I_E = 5$ ma, $V_{CE} = 10$ v)

| Frequency (Mc) | Parameter (mmho) | | | |
|-------------------|------------------|-----------------|--------------|----------------|
| | y_{11} | y_{12} | y_{21} | y_{22} |
| 10 | $1.7 + j0.65$ | $-0.01 - j0.07$ | See Footnote | $0.08 + j0.13$ |
| 50 | $2.5 + j2.5$ | $0.0 - j0.3$ | $80 - j60$ | $0.1 + j1$ |
| 100 | $5 + j5$ | $0.0 - j0.7$ | $40 - j60$ | $0.2 + j1.3$ |
| 200 | $8 + j8$ | $0.0 - j1.3$ | $25 - j55$ | $0.5 + j2.5$ |
| 300 | $10 + j10$ | $-0.1 - j2$ | $15 - j47$ | $0.6 + j3.5$ |
| 400 | $12 + j12$ | $-0.2 - j2.7$ | $7 - j43$ | $0.8 + j4.5$ |
| 500 | $17 + j14$ | $-0.4 - j3.4$ | $0.0 - j40$ | $1 + j6$ |

* $|h_{21}| = 62.5$ at 10 Mc.

2. Determining the Feedback Circuit

Figure 18 contains, in the Y_F plane, the constant power-gain circles for $Y_K = 20$ mmho and for a very low frequency (10 Mc). These circles correspond to $p = 9, 10, 11$ and 12 db. Also contained in the Y_F plane are the constant (P_{O0}/P_{I0}) circles for $f = 400$ Mc. Considering the intersections of these circles, it is seen that $p = 11$ db could be chosen, but since the transistor y parameters specified in Table 4 are merely typical parameters, p is chosen to be 10 db. It is to be noted further that in Fig. 18 there are two intersections of the 10-db

circles, thus yielding two solutions for the normalized feedback impedance:

$$Z_F \text{ norm} = 0.7 + j5.0 \quad (27)$$

and

$$Z_F \text{ norm} = 0.7 + j0.5$$

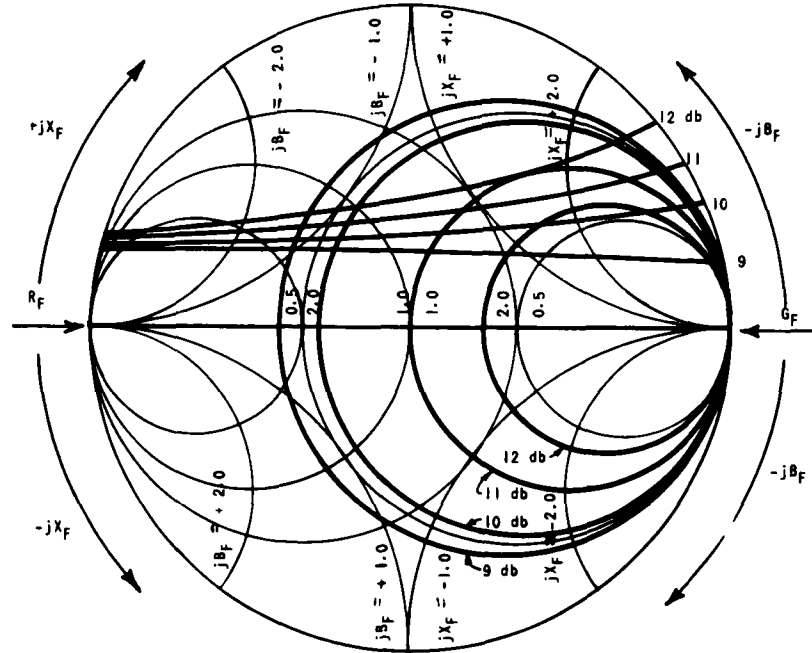


FIG. 18. THE Y_F PLANE (NORMALIZED TO 5 mmho). $Y_K = 20$ mmho; $f = 400$ Mc; $11 \text{ db} < p_{\text{max}} < 12 \text{ db}$. Choosing $p = 10 \text{ db}$ gives $Z_F = 0.7 + j0.5$ or $Z_F = 0.7 + j5.0$.

In order to preserve midband gain, $Z_F \text{ norm} = 0.7 + j5.0$ is chosen.

$$Z_F = (0.7 + j5.0) \times 200 = 140 + j1000 \text{ ohms} \quad (28)$$

$$R_F = 140 \text{ ohms} \quad (29)$$

$$L_F = 0.4 \mu\text{h}$$

The feedback admittance $Y_F(f)$ is calculated from the foregoing values for R_F and L_F , and the results are listed in Table 5.

TABLE 5. VARIATION OF Y_F WITH FREQUENCY

| Parameter | Frequency (Mc) | | | | |
|----------------------|----------------|-----------|-----------|------------|-----------|
| | 50 | 100 | 200 | 300 | 400 |
| $Y_F(\text{norm})^*$ | 0.8-j0.7 | 0.35-j0.6 | 0.1-j0.37 | 0.05-j0.25 | 0.03-j0.2 |
| $Y_F(\text{mmho})$ | 4 -j3.5 | 1.75-j3.0 | 0.5-j1.85 | 0.25-j1.25 | 0.15-j1.0 |

* Normalized to 5 mmho.

3. The Constant-g Circles

The y parameters of the transistor with its feedback circuit connected (Table 6) can now be determined.

TABLE 6. THE y PARAMETERS OF THE TRANSISTOR WITH
FEEDBACK CIRCUIT CONNECTED
 $[y](f) = [y_T](f) + [y_F](f)$

| Frequency (Mc) | Parameter (mmho) | | | |
|-------------------|------------------|---------------|----------|-------------|
| | y_{11} | y_{12} | y_{21} | y_{22} |
| 10 | --- | --- | --- | --- |
| 50 | 6.5 - j1.0 | -4.0 + j3.2 | 76 - j57 | 4.1 - j2.5 |
| 100 | 6.75 + j2.0 | -1.75 + j2.3 | 38 - j57 | 2.0 - j1.7 |
| 200 | 8.5 + j6.15 | -0.5 + j0.6 | 25 - j53 | 1.0 + j0.65 |
| 300 | 10.3 + j8.8 | -0.35 - j0.75 | 15 - j46 | 0.9 + j2.3 |
| 400 | 12.2 + j11 | -0.35 - j1.7 | 7 - j42 | 1.0 + j3.5 |

On the LM plane, the constant-g circles for $f = 100, 200, 300$, and 400 Mc are plotted in Fig. 19 using the following relationships:

$$x^2 + y^2 = 1 - g(1 + Cx) \quad (30)$$

$$g = \frac{(P_o/P_1)}{(P_{o0}/P_{i0})} = \frac{p}{(P_{o0}/P_{i0})} \quad (31)$$

$$\Delta g = \frac{\Delta p}{(P_{o0}/P_{i0})} \quad (32)$$

In the present situation, $p = 10$ (10 db) and $\Delta p = 1$ db.

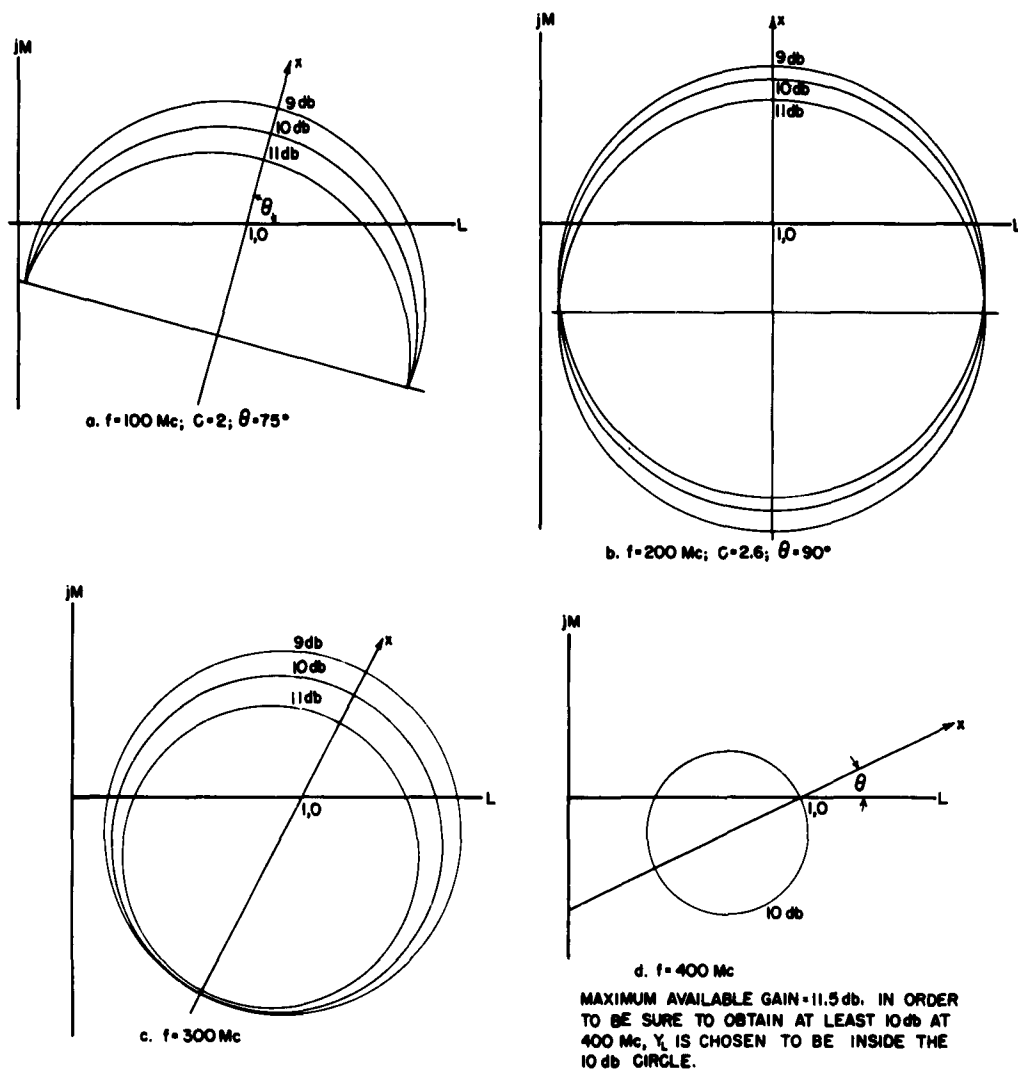


FIG. 19. THE CONSTANT-g CIRCLES.

4. The Constant- ρ Circles

With $\rho = 1/3$, the insertion power loss is less than 0.5 db. The constant- ρ circles and the constant-g circles are plotted in Fig. 20, using Smith-chart coordinates for γ_L .

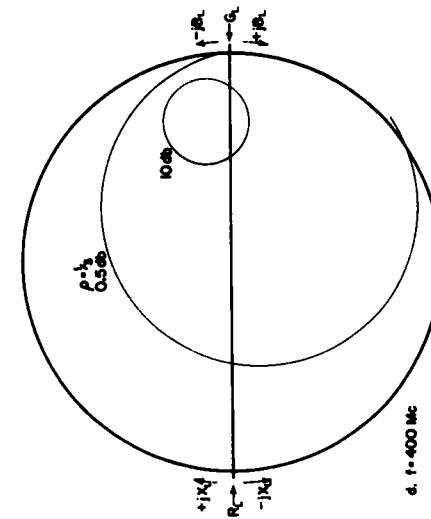
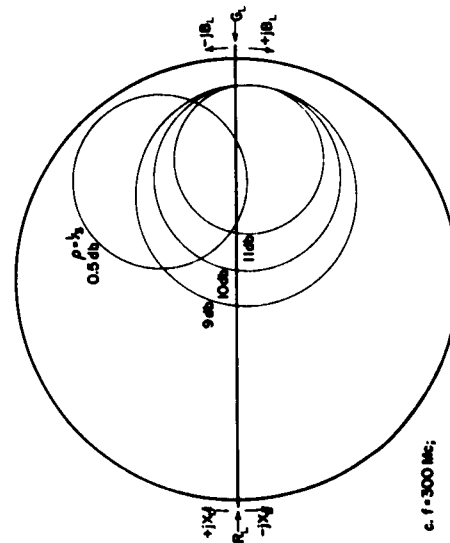
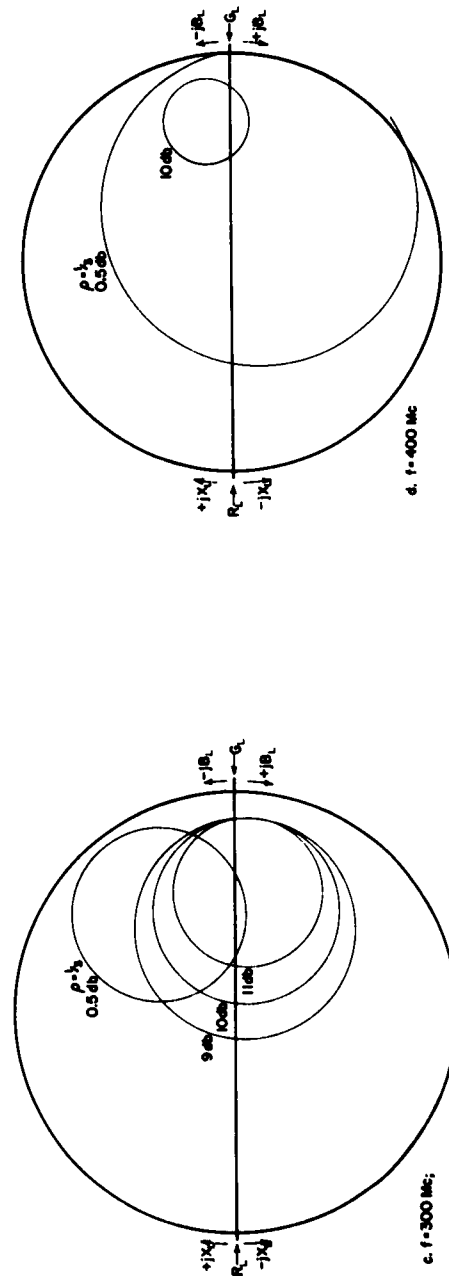
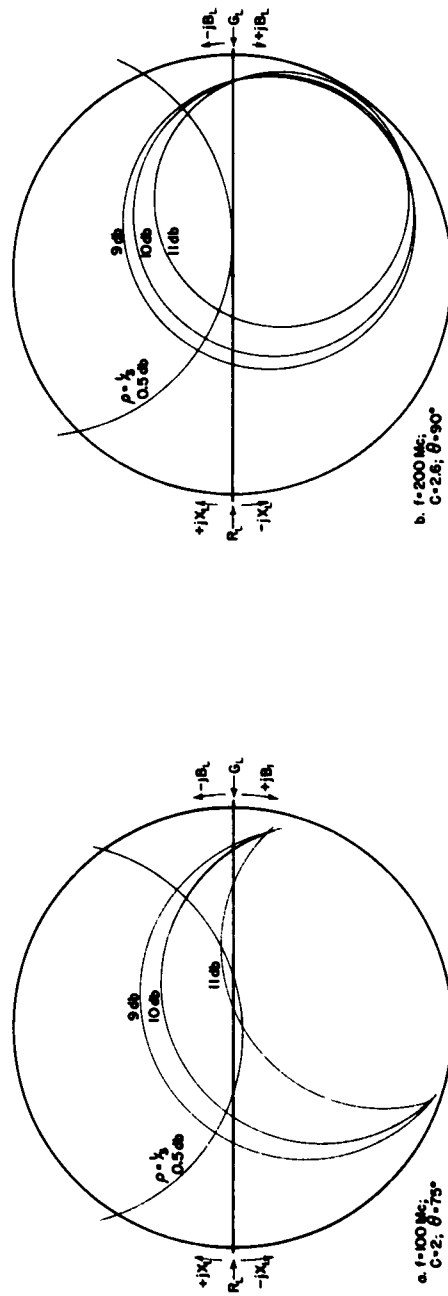


FIG. 20. FINDING THE Y_L LOCATION.

5. The Interstage Network

A few investigations lead to the two-port shown in Fig. 21.* The input admittance of this two-port, when loaded with Y_K , falls into the regions determined in Fig. 20.

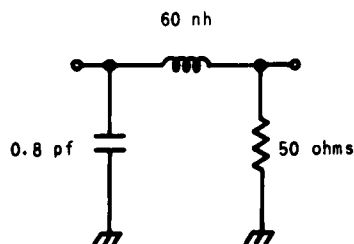


FIG. 21. THE INTERSTAGE NETWORK
FOR THE 400-Mc AMPLIFIER.

B. BRIDGE MEASUREMENTS

After arriving at design values for the individual circuit elements, the following bridge measurements are made: **

1. Measurements of the transistor y parameters,
2. Measurements of the y parameters of the transistor with feedback circuit connected, adjusting the feedback circuit so that the parameters approach the design values as closely as possible, and
3. Measurements of the y parameters of the complete stage, consisting of transistor, feedback circuit, and interstage network. During these measurements the interstage inductor can be adjusted so that the y parameters of the complete circuit correspond to an iterative structure with a characteristic impedance of 50 ohms and an insertion gain of 10 db.

* For an extensive discussion of the design of coupling networks, see Chap. 14 of Transistors and Active Circuits, by Linvill and Gibbons [Ref.6].

** A General Radio 1607-A Transfer-Function and Immittance Bridge was used for these measurements during the realization of the 400-Mc amplifier described in this report.

During the course of these measurements and adjustments, it is helpful to keep in mind the fact that, at high frequencies, the circuit elements behave like distributed rather than lumped elements.

C. PRACTICAL DATA

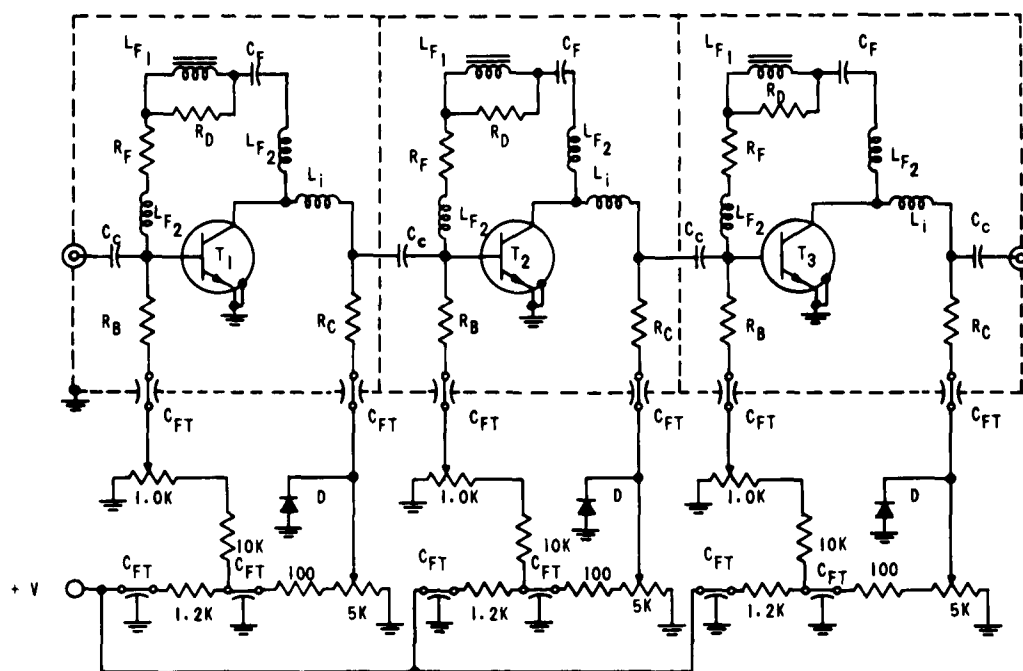
A detailed schematic circuit of the 400-Mc amplifier realized by the foregoing methods is shown in Fig. 22. Slight adjustments of the emitter currents were used to improve the response shape. In order to permit transistor interchangeability, voltage and current adjustments were provided for each stage.

Figure 23 is a photograph of the amplifier. Shields were used between stages, each emitter was grounded with a very short connection, and each transistor case was grounded. Stand-off insulators and transistor sockets were avoided, except for a teflon stand-off insulator used at the base of the input transistor. The base leads of the second and third transistors were connected directly to 50-ohm bulkhead female microconnectors in order to permit optional independent connection to any one of the individual stages.

D. FINAL SUMMARY OF AMPLIFIER PERFORMANCE

Figures 24 through 31 summarize the performance of the 400-Mc amplifier. From these figures it can be seen that the three-stage amplifier has a gain of 30 db, a rise time of 1 nsec, and an overshoot of less than 10 percent.

The three original transistors were replaced by three others. Slight modifications of the emitter currents made it possible to regain the original amplifier characteristics, the adjustment process being rapidly "convergent" when carried out using a sweep-frequency generator. Although such a single trial cannot be considered conclusive, it indicates that the amplifier might be reproducible on a production basis.



- R_B - I.R.C. "HFR" HIGH-FREQUENCY RESISTORS, 2.2K, 1/4 w
 R_C - I.R.C. "HFR" HIGH-FREQUENCY RESISTORS, 1.0K, 1/4 w
 R_D - I.R.C. "HFR" HIGH-FREQUENCY RESISTORS, 270 OHMS, 1/4 w
 R_F - I.R.C. "HFR" HIGH-FREQUENCY RESISTORS, 150 OHMS, 1/4 w
 L_i - 7 TURNS NO. 20 AWG SOLID TINNED WIRE, 1" LONG, 5/32" INSIDE DIAMETER
 L_{F1} - 5-1/2 TURNS NO. 20 AWG SOLID TINNED WIRE IN TEFLON SLEEVE WOUND ON GENERAL CERAMICS TOROID
 *CF103 (1/2" OD x 9/32 ID x 3/32" THICK), Q-3 MATERIAL
 L_{F2} - 6 TURNS # 20 AWG, SOLID TINNED WIRE, 19/32" LONG x 5/32" INSIDE DIAMETER
 C_C - 0.01 μ f CERAMIC DISC CAPACITORS
 C_F - 0.01 μ f CERAMIC DISC CAPACITORS
 C_{FT} - CERAMIC FEED-THROUGH CAPACITORS - 1500 pF
 D - AVALANCHE PROTECTIVE DIODE TYPE 1N720, 18 v NOMINAL BREAKDOWN
 T_1, T_2, T_3 - FAIRCHILD 2N918

FIG. 22. SCHEMATIC CIRCUIT OF THE 400-Mc AMPLIFIER.

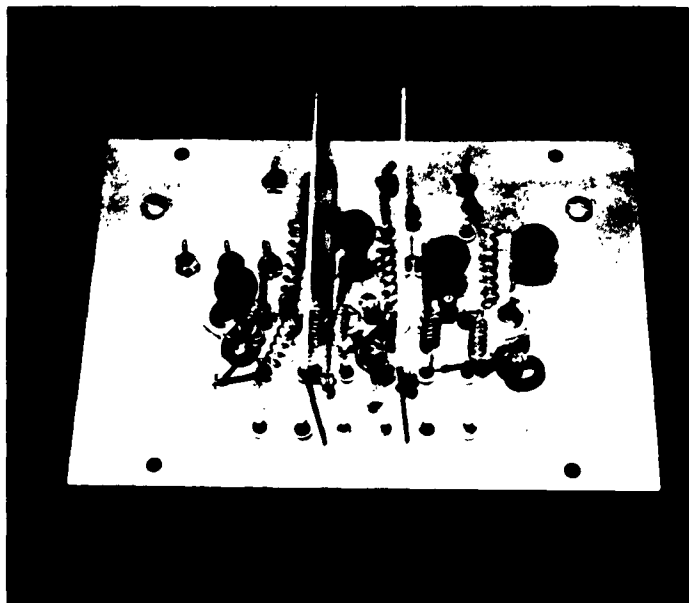


FIG. 23. PHOTOGRAPH OF THE 400-Mc AMPLIFIER.

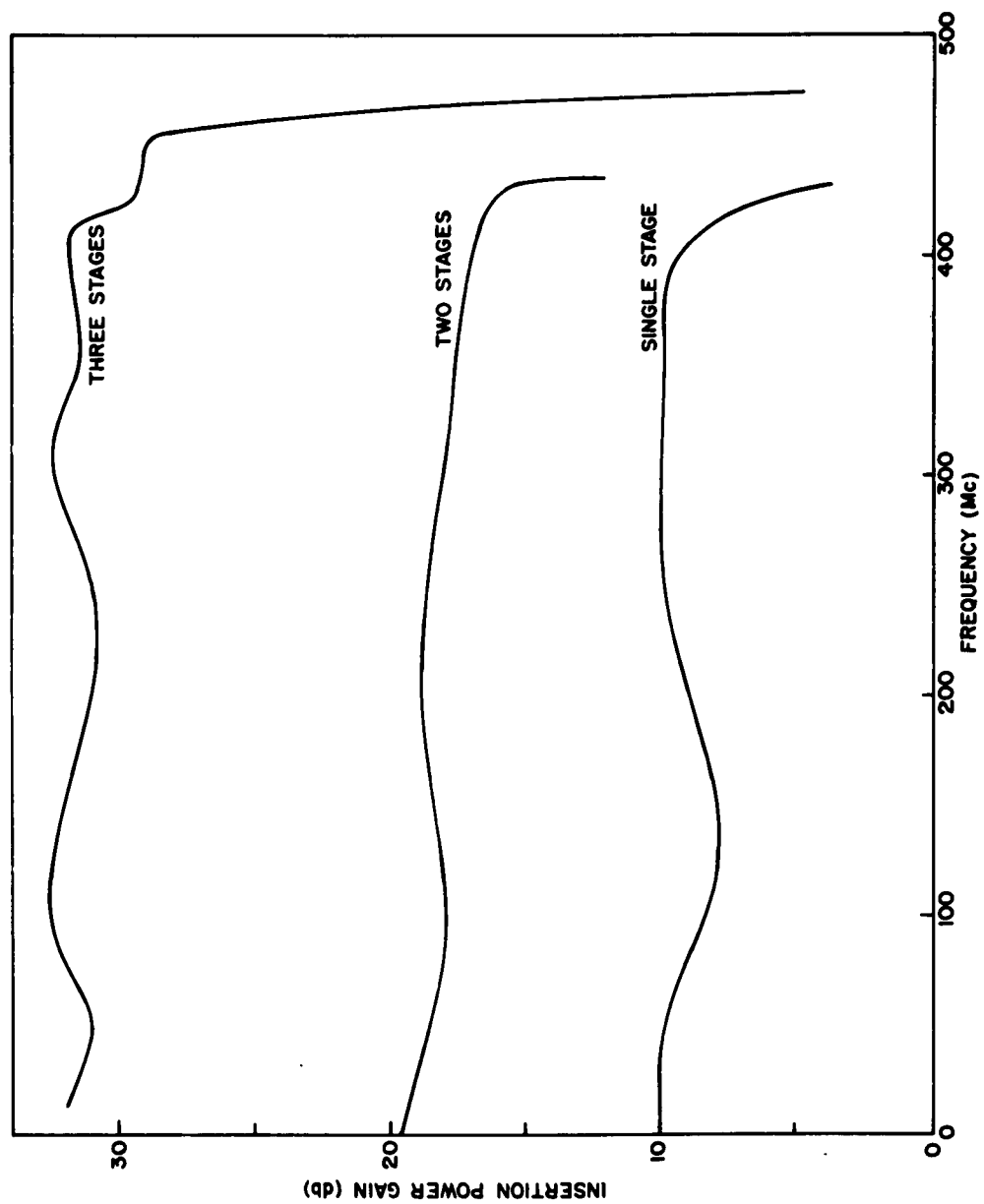
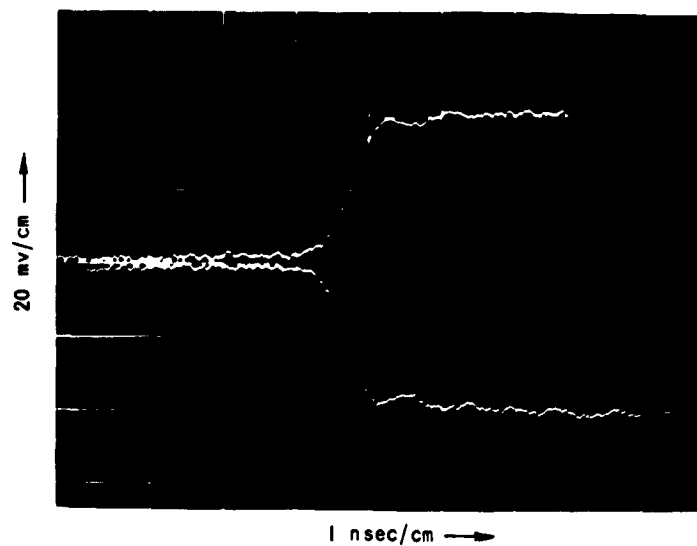
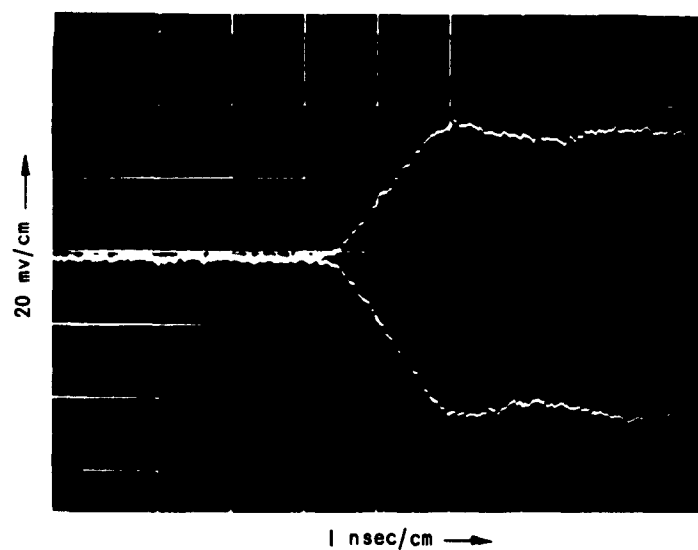


FIG. 24. INSERTION POWER GAIN VS FREQUENCY.

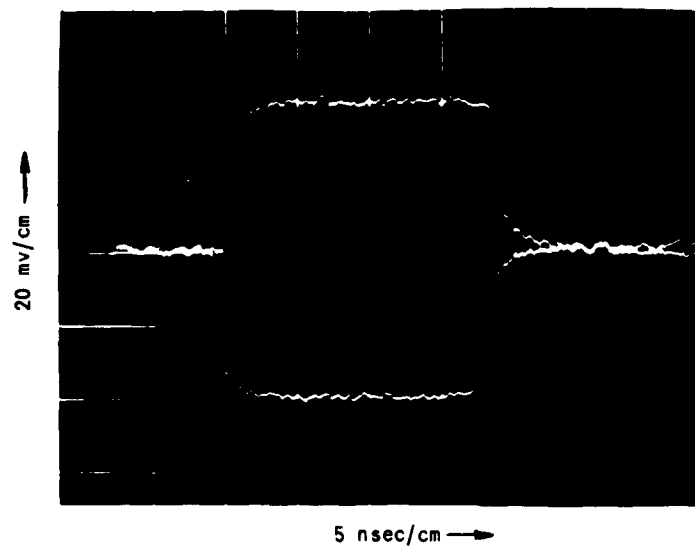


a. Input step

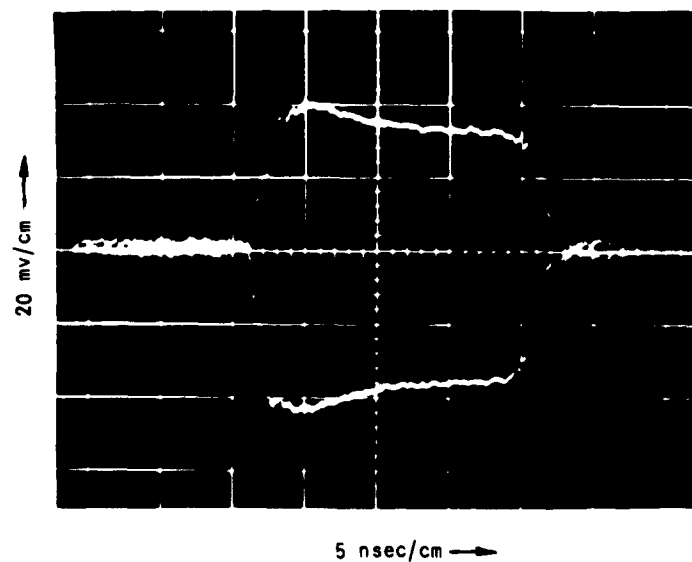


b. Output step for amplifier plus 10-db attenuator.

FIG. 25. STEP RESPONSE OF THE SINGLE-STAGE AMPLIFIER.



a. Input pulse



b. Output pulse for amplifier plus 10-db attenuator.

FIG. 26. PULSE RESPONSE OF THE SINGLE-STAGE AMPLIFIER.

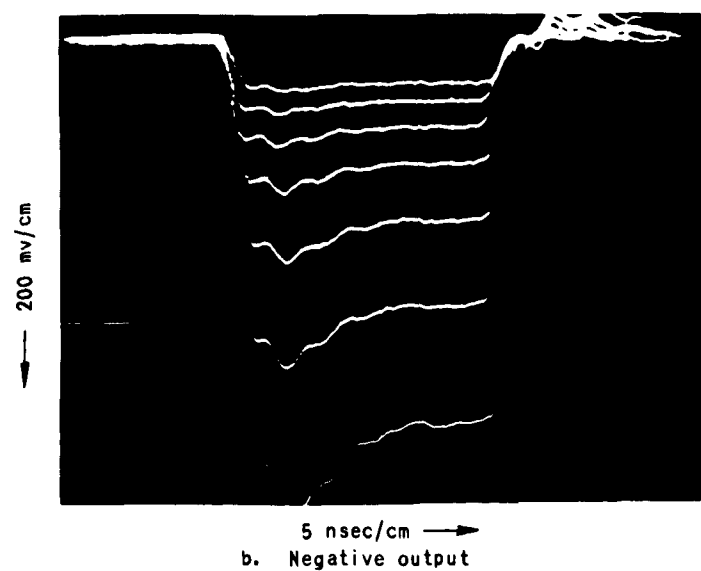
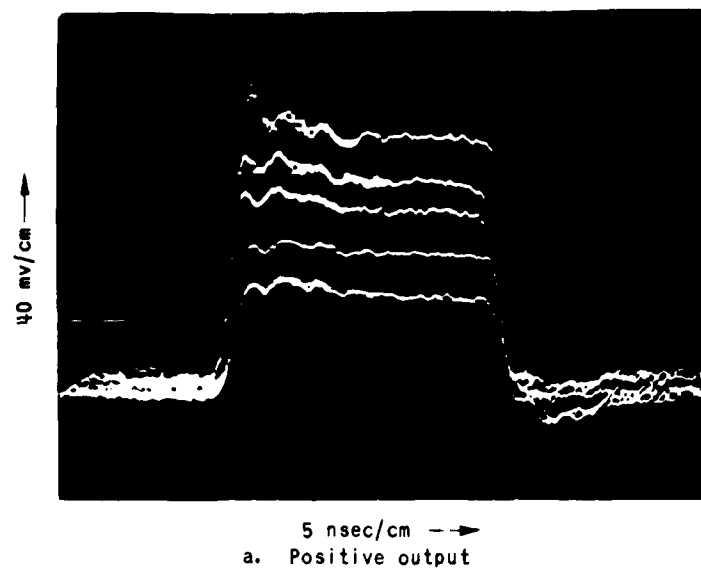


FIG. 27. DYNAMIC RANGE OF THE SINGLE-STAGE AMPLIFIER. Input pulse varied in 3-db increments in both (a) and (b).

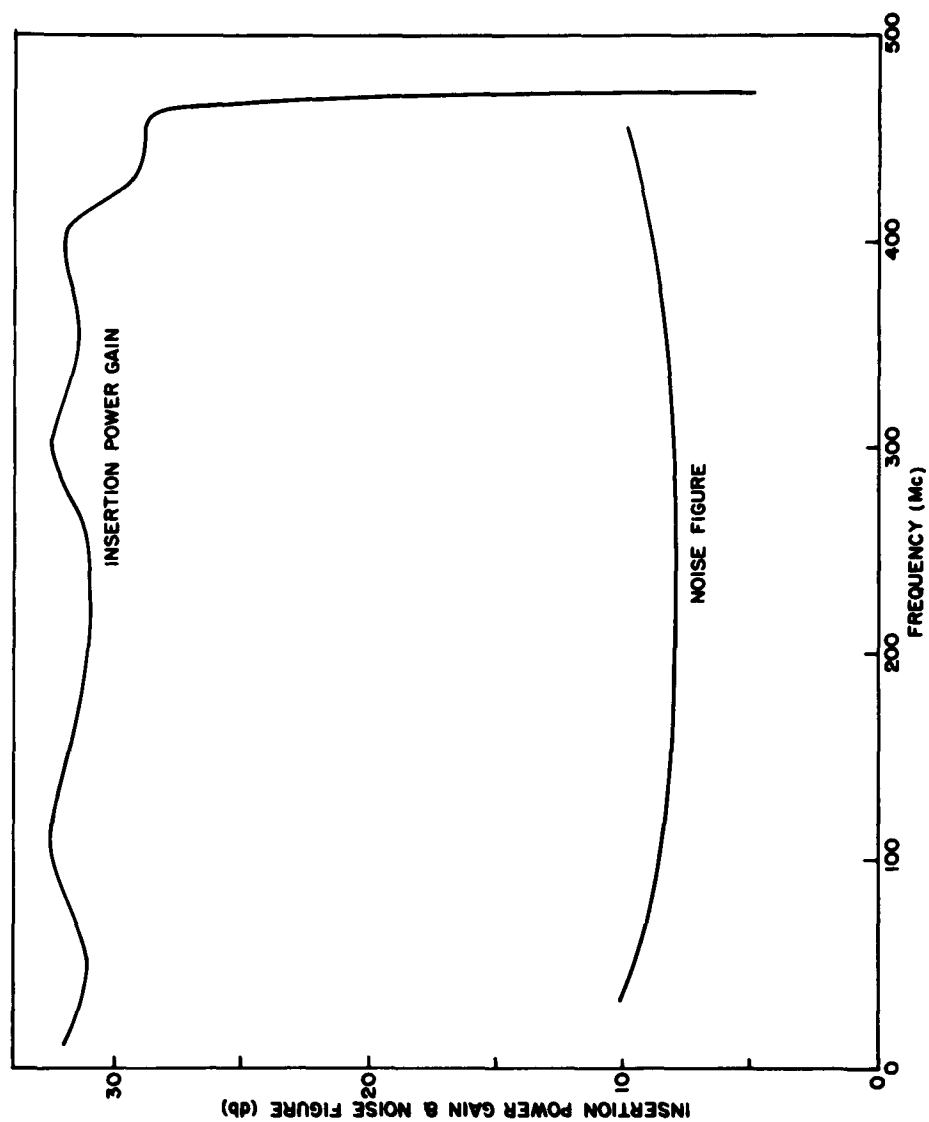
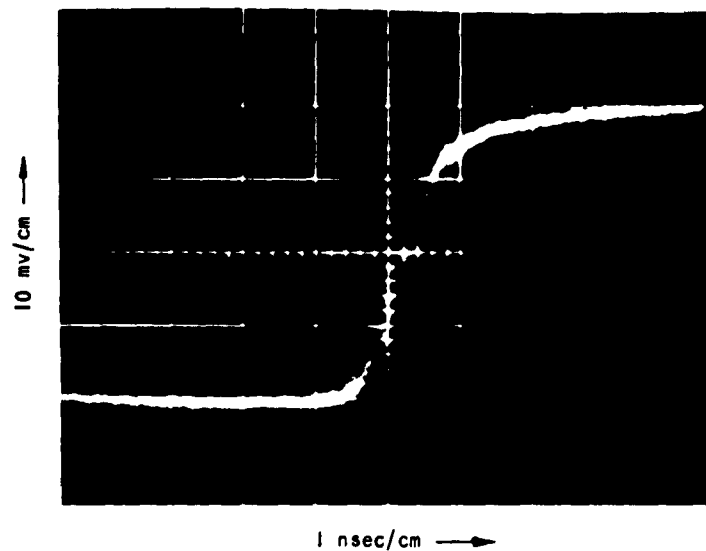
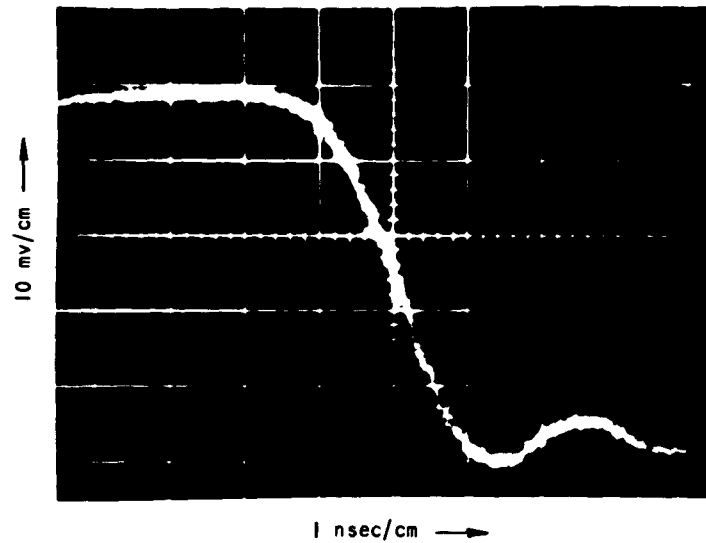


FIG. 28. INSERTION POWER GAIN AND NOISE FIGURE VS FREQUENCY FOR THE THREE-STAGE AMPLIFIER.

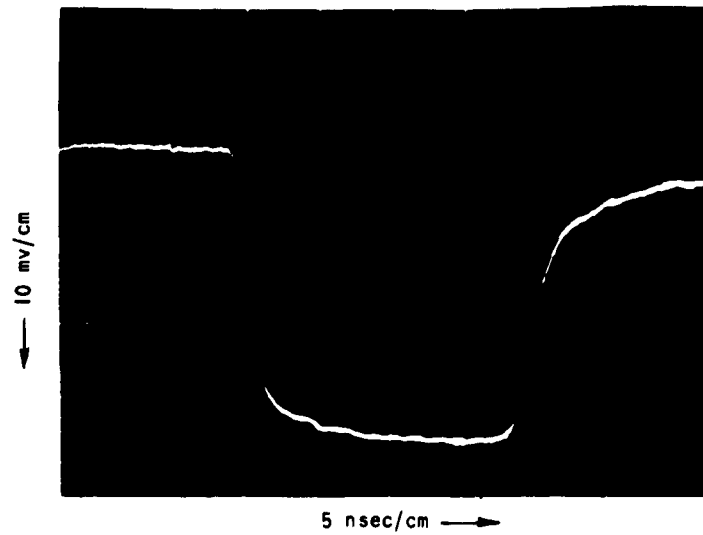


a. Input step

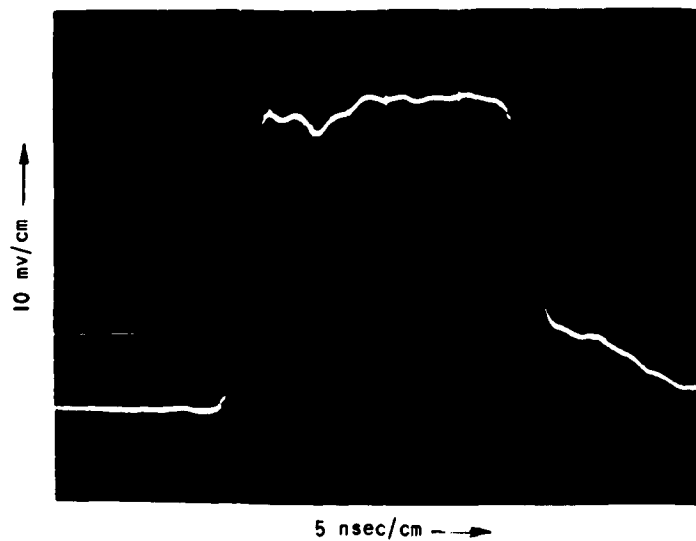


b. Output step for amplifier plus 30-db attenuator

FIG. 29. STEP RESPONSE OF THE THREE-STAGE AMPLIFIER.

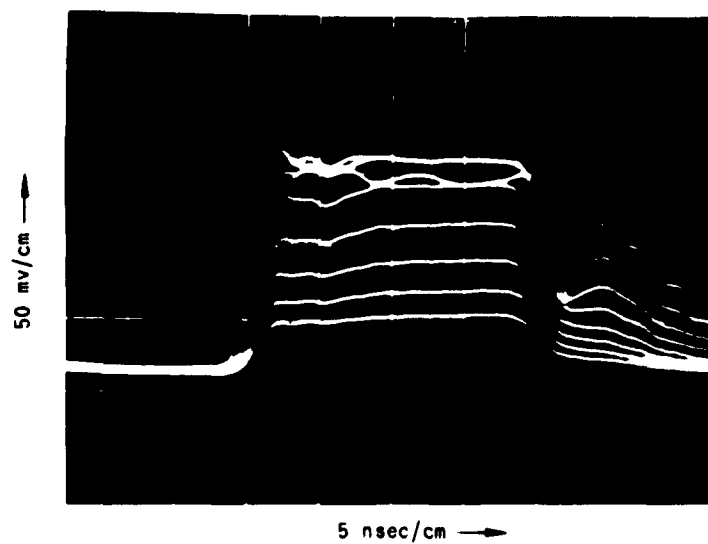


a. Input pulse

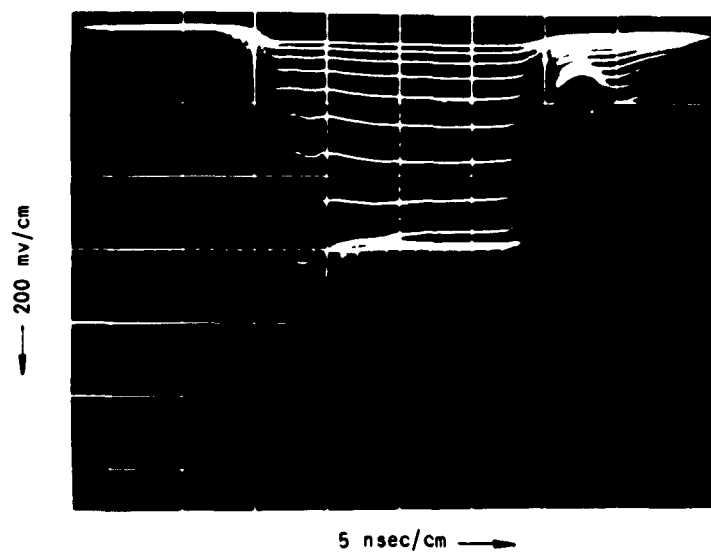


b. Output pulse for amplifier plus 30-db attenuator

FIG. 30. PULSE RESPONSE OF THE THREE-STAGE AMPLIFIER.



a. Positive output pulse for 8 values of input pulse differing in amplitude by 3 db



b. Negative output pulse for 11 values of input pulse differing in amplitude by 3 db

FIG. 31. DYNAMIC RANGE OF THE THREE-STAGE AMPLIFIER.

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